OVERVIEW OF THE CSNS LINAC LLRF AND OPERATIONAL EXPERIENCES DURING BEAM COMMISSIONING

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Abstract

The CSNS proton linear accelerator (Linac) will deliver 81MeV proton beam to RCS ring. The Linac is comprised of H- ion source, RFQ, two Buncher cavities (MEBT), four DTL accelerators and one Debuncher cavity (LRBT). The RFQ accelerator is powered by two 4616 tetrodes, the maximum output power of each tube is 350kW. Three 25kW solid state amplifiers supply RF power to two Buncher cavities and one Debuncher cavity, repectively. The RF power sources of four DTL accelerators are four 3MW klystrons. Each RF power source owns a set of digital LLRF control system in order to realize an accelerating field stability of ±1% in amplitude and ±1° in phase. The front four LLRF control systems have been used in the beam commissioning of CSNS Linac in the end of 2015. This paper will introduce the design and the performance of the digital LLRF control system.

INTRODUCTION

In the CSNS 81MeV proton linear accelerator (Linac), the RF power sources consist of two 350kW 4616 tetrodes, three 25kW solid state amplifiers, five 3MW klystrons (including spare one). Now, the 4616 tetrodes, two solid state amplifiers and the first Klystron power source have already supplied RF power to the corresponding accelerating cavities for the ageing process and beam commissioning. The installation and test of the rest three klystron power sources are still in process. The block diagram of the Linac RF system is shown in Figure 1 [1].

The RF field are controlled by eight almost the same digital LLRF controllers which are installed in cabinets. The prototype of the digital LLRF control system was developed in the 352MHz RFQ of IHEP, the design team have gathered much experiences from the operating process of the prototype. Based on the good design experiences of the prototype, the improvement and commissioning of the eight on-line LLRF hardwares are completed quickly, software algorithms are also completed with some elaborate improvements on time.

As shown in Figure 2, each LLRF control system consists of the 324MHz RF reference line, analog module (AM) and clock distribution module (CDM), digital control module (DCM) and the high power protection module (HPM). Because the AM and CDM are absolutely analog components, most analog components are susceptible to ambient temperature, so we put these two modules into a temperature stabilizing chamber. The DCM is mainly responsible for the stability of the RF field amplitude and phase, HPM can quickly cut off the RF drive in case of arc in the RF distribution system, VSWR over threshold or cavity vacuum fault, and so on. The field control algorithms and high power protection logics are designed through digital signal processing in FPGA and DSP. Various control parameters can be set from IPC human-computer interface through embedded Ethernet communication. The block diagram of the digital LLRF control system is showed in Figure 2.
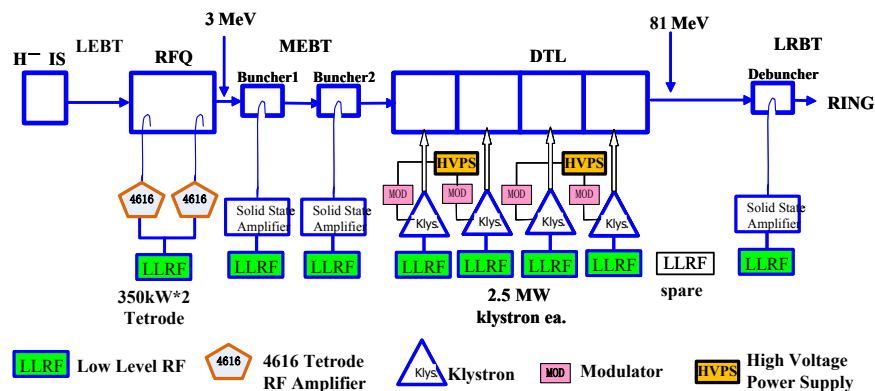

Figure. 1: Block diagram of the CSNS Linac RF system.
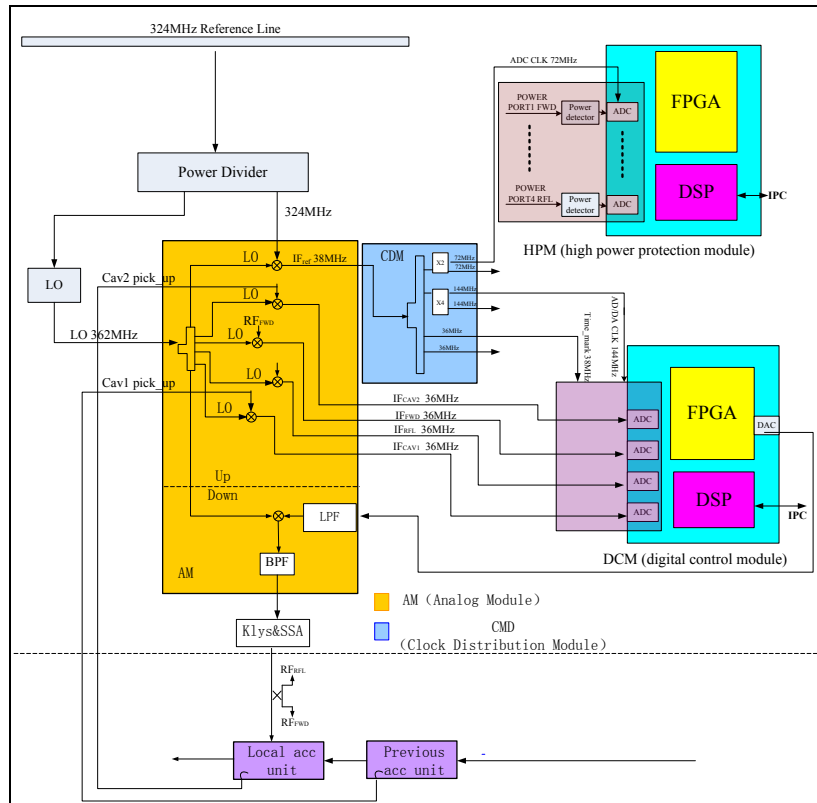
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Figure 2: Overview of the digital LLRF control system.

THE 324MHz REFERENCE LINE [2]

The 324MHz reference signal of the Linac is from the reference line system, and the reference signal is from the main oscillator, the reference line stretches along the sub-tunnel of CSNS Linac, Figure 3 shows the whole structure of the sub-tunnel. The phase stable cable is wrapped in a constant temperature water jacket, the variation range of the water temperature is limited within $\pm 0.1°$. The reference signal is picked up through a Narda 3000 coupler, and transferred to each LLRF station through Andrew phase stable cable.

Figure 3: The 324MHz reference line of the CSNS Linac.

THE AM AND CDM

As shown in Figure 2, the AM consists of four down conversion channels and two up conversion channels, The frequencies of the LO and IF are 360MHz and 36MHz, respectively. The clocks distribution module generates three clocks: 144MHz, 36MHz and 72MHz. The 144 MHz and 36MHz clocks are used as the 4 channel ADC sampling clock of the DCM, and 72MHz clock is used as the 8 channels ADC sampling clock of the HPM. In order to achieve the higher control precision of the RF filed amplitude and phase, the analog up-down conversion unit and the clocks distribution module are put into a temperature stabilizing chamber, as shown in Figure 4, the two units are installed parallel inside the chamber, it adopts the air cooling semi-conductor refrigeration technology to keep the temperature stable. The temperature variation range inside chamber is less than $\pm 0.1℃$.

Figure 4: Temperature stabilizing chamber.

HIGH POWER PROTECTION MODULE (HPM)

The high power protection module owns eight power detector channels, as shown in Figure 5, the power detector array are installed in the chassis beside the HPM digital signal processing board. The forward/reflected RF signals which are picked up by the directional couplers along power transmission line are sent into the power detector channels, and the DC pulses are sampled by 72MHz ADCs, the high power VSWR protection logics are realized in FPGA. The maximum protection threshold of the VSWR can be set in IPC through human-computer interface, and the RF switch will cut off the the RF drive in case of VSWR over set value. Total VSWR interlock number during the accelerator operating period is recorded in database. The arc sentry and the fiber probes are purchased from AFT, the arc protection logics are also designed in FPGA.

Figure 5: Power detector array of the HPM.

INTRODUCTION OF THE DIGITAL FEEDBACK CONTROL

The picture of the digital feedback control board is shown in Figure 6, the mother board of the digital feedback controller consists of a Stratix II FPGA and two TI C6713 DSPs, ADC sampling daughter board with four AD sampling channels is mounting on the mother board.

Figure 6: Digital feedback control board.

The frequency of the ADC sampling clock is 144MHz, the forward/reflected RF signals and the cavity pick-up signal are down-converted to 36MHz IF signals by mixers, the digital I, Q, -I, -Q sequences of the three IF signal are sent into FPGA, the I, Q components of the forward/reflected RF signals is just used to calculate the phases which are the judgment basis of the cavity detuning. The I and Q components of the 36MHz cavity pick-up signal are produced by sampling it with 144MHz clock, then a series of digital signal processing is performed, including rotational matrix, digital PI controller and NCO, etc. Reference tables of the feedback control loop can be set from IPC, one is step mode, the other is exponential mode. The FB ON and OFF can be set in the human-computer interface in IPC. If the FB is off, the reference table will drive the RF power source directly, otherwise, the digital feedback control loop begins to take effect. The feedback loop suppresses various disturbances including the power sources noises, high voltage drop, beam loading, and so on. In actual operating, we gradually increase the Kp, Ki parameters as long as the oscillation doesn't appear.

A fixed feedforward table is used to compensate the beam loading effect, and the feedforward compensation is triggered by the synchronous beam pulse, we can adjust the delay time of the pulse, make the feedforward driving precisely synchronized with the beam loading in cavity. The fixed value of the table can be adjusted in IPC. After the feedback and feedforward process, I/Q components are finally sent into numerically controlled oscillator (NCO), NCO outputs the 36MHz digital IF signal.

THE DIGITAL FREQUENCY CONVERSION TECHNOLOGY FOR WARM-UP CAVITY

The digital frequency conversion technology tunes the output frequency of the power sources to match the RF cavities during the RF start-up. It is carried out by NCO IP core in FPGA, by using this technology, the RF start-up time in cavity obviously decreased, the cavity field building process is quickly and smoothly.

Two types of frequency conversion mode can be selected, the auto frequency conversion mode and the manual mode. In the auto-mode, we calculate the detuned frequency from the operating frequency of the cavity by the phase decay curve during the damped oscillation after the end of RF pulse [3].

$$\Delta\omega = \frac{\partial \theta}{\partial t}$$

Then we change the frequency of the NCO sine and cosine function according to the $\Delta\omega$, output frequency of the RF power source will be consistent with the resonant frequency of the cavity, and the RF power can be fed into the cavity quickly with less reflected power. The RF pulse waveform of the power source output is shown in Figure

7, and the amplitude modulation results from the mechanism of frequency conversion.
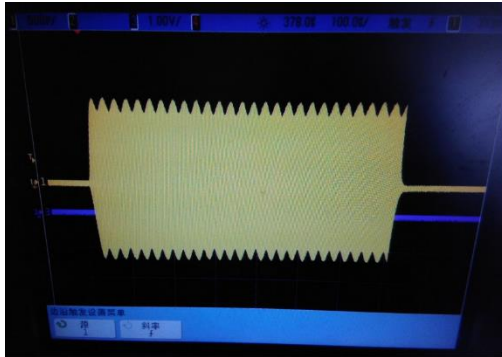

Figure 7: RF pulse waveform with frequency conversion.

PERFORMANCE OF THE DIGITAL FEEDBACK CONTROL

The hardware installation and software development of the eight LLRF control system is completed, the LLRF systems of RFQ, two Buncher cavities and DTL1 have been used in the high power ageing process and the beam commissioning. As previously mentioned in the abstract, the required performance of the cavity field error is less than ±1% in amplitude and ±1° in phase, according to the actual operating experiences, the control precision satisfies the specified performance, Figure 8 shows the control results of the cavity field in RFQ, we can see that a good stability of the RF field has been achieved about $\pm 0.4\%$ in amplitude and $\pm 0.5°$ in phase when the amplitude is set to 6270 and the phase is set to 0°, and the pulse width of the RF is 700μs, beam width 500μs, beam intensity 10mA.
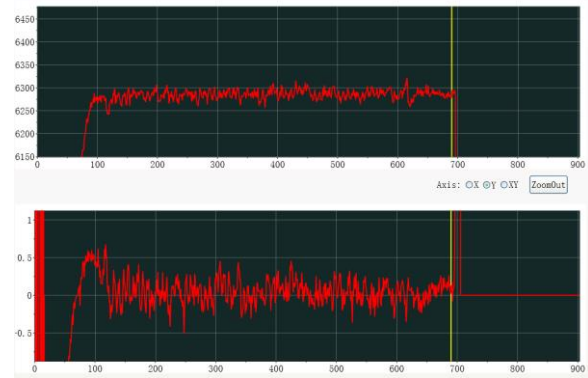

Figure 8: Performance of the LLRF control system in RFQ.

SUMMARY

Next, we will complete the debug of the rest LLRF control systems, and the long term stability of the LLRF system still need time to test. We want to improve it with chassis and CPU in the future, the cPCI chassis with Vxworks OS will be a choice.

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